

REMARKS

Applicants appreciate the thorough review of the present application that is reflected in the previous Office Actions, and the allowance of Claims 12-16 and 18-31. Applicants likewise appreciate the indication that Claims 7-11 are directed to allowable subject matter.

I. New Claims 46-49

In the Amendment mailed October 12, 2005, Applicants added new dependent Claims 46-49 to the present application. Each of these claims is directed to the invention elected in response to the Restriction Requirement issued in this case. New dependent Claims 46-49 were not discussed in the December 12, 2005 Office Action. As each of these new dependent claims depends either directly or indirectly from Claims 7, 8 or 9 – each of which are directed to allowable subject matter – Claims 46-49 should be in condition for allowance except for depending from a rejected base claim. In any event, Applicants respectfully request that the Examiner expressly address Claims 46-49 in all subsequent proceedings.

II. The Rejections of Claims 1, 3, 5 and 6

Claims 1, 3, 5 and 6 stand rejected as anticipated by U.S. Patent No. 5,637,903 to Liao et al. ("Liao"). Claim 1 recites:

1. A semiconductor device, comprising:
a gate electrode on a semiconductor substrate, the gate electrode including a metal silicide layer on a polysilicon layer and extending in a first direction; and
a conductive line pattern extending in the first direction and being in contact with the gate electrode along the first direction.

One embodiment of such a semiconductor device is disclosed in Figs. 3-5 of the present application. As shown in these figures, a gate line 108 (that includes a gate electrode 107) and a conductive line pattern 120a extend in the same direction to cross over a plurality of active regions 103 and isolation regions 102. In contrast, the semiconductor device depicted in Liao discloses a device that includes a gate structure 4, 8. (Liao at Col. 4, lines 1-7 and FIGS. 4-5). A "via 14" (i.e., a contact hole) is provided above each gate

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structure, and then filled with Al-Cu-Si metallization to form metal contacts 15 to the polysilicon gates 4. (Liao at Col. 4, lines 38-49 and FIG. 5). Liao further states that "[v]ia holes are also made to the source and drain regions (not shown)." (Liao at Col. 4, lines 42-43).

As made clear above, the metal contacts 15 of Liao are provided in conventional via holes. As such, Liao does not disclose or suggest either (1) a "conductive line pattern" as recited in Claim 1 or (2) a semiconductor device that includes "a gate electrode . . . extending in a first direction" and "a conductive line pattern extending in the first direction" as recited in Claim 1. Consequently, Applicants respectfully submit that Claim 1 is patentably distinct over Liao for at least each of the above reasons, and that therefore the rejection of Claim 1 should be withdrawn. As Claims 3, 5 and 6 each depend from Claim 1, the rejections of these claims should likewise be withdrawn. Applicants note that dependent Claim 6 has been amended.

III. Conclusion

Applicants submit that the present application is now in condition for allowance, which is respectfully requested.

Respectfully submitted,



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